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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,114	10/22/2001	Tai-Peng Lee	M-11912 US	7687

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EXAMINER	
GARCIA, JOANNIE A	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,114	LEE ET AL.	
	Examiner	Art Unit	
	Joannie A García	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,44-52* is/are allowed.

6)☒ Claim(s) *1-10,12-43 and 53-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 12-43, and 53-58, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (U.S. Patent 6,291,030), in combination with Liu et al (U.S. Patent 6,211,040), and the following comments.

Chao et al discloses using oxygen and silane gases to reactively form, deposit, and resputter silicon dioxide 403/501/601 in substrate 407 by a HDP-CVD process for deposition into at least two trenches of different aspect ratios and widths, wherein a first trench is at least twice as wide a second of the trenches (Figure 5, Column 2, lines 65-67, and Column 3, lines 1-15, and 40-43), using ions to sputter etch a portion of the formed silicon dioxide during the deposition so as to fill the trenches with the formed silicon dioxide (Figure 5, Column 2, lines 65-67, and Column 3, lines 1-15), controlling the sputter etch and deposition of the silicon dioxide such that a nonzero etch to deposition ratio ranges from is 0:01 to 0.1 is established during the filling of said different trenches, wherein a 0.07, 0.025 or less etch to deposition ratio could be selected (Column 3, lines 40-43), overfilling the at least two trenches with the deposited silicon dioxide, and using CMP to remove at least a portion of the overfilling silicon dioxide (Figure 6, and Column 3, lines 62-64). Chao et al discloses as well, depositing the silicon dioxide layer over an electrically conductive layer used as a metal interconnect 401 (Abstract, Figure 5, Column 2, lines 45-46, and 51-52, and Column 3, lines 1-4, and 40-50).

Chao et al discloses a monolithically integrated device having a semiconductor-containing substrate and plural trenches defined to extend into at least one layer 401 of the device to substantially same depths (Figures 4 and 5), where at least a first and second of said same-depth trenches respectively have different widths, the width of the second trench being at least twice the width of the first trench (Figures 4 and 5), said integrated device being further characterized by said same depth trenches of different widths are each filled with a silicon oxide 403/501/601 deposited by way of HDP-CVD to substantially same heights above said substantially same depths to thereby provide a substantially planar set oxide-filled trenches upon which other layers of material are founded (Figures 5 and 6), wherein the height of said oxide-filled trenches lie adjacent to silicon regions (Figure 5).

Chao et al discloses using oxygen, silane and inert gas to deposit a silicon oxide layer 501 over metal interconnect 401 by an HDP-CVD process (Abstract, Figure 5, Column 2, lines 45-46, 51-52, and 65-67, and Column 3, lines 40-50), and controlling a bias signal which affects a sputter etch action of the inert gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which ranges from is 0.01 to 0.1 is established during the filling of said different trenches, wherein a 0.075, 0.07, 0.025 or less etch to deposition ratio could be selected (Column 3, lines 40-43). Chao et al does not teach using an oxygen inflow rate to silane inflow rate ratio of 1.7, 1.3 or less, using a total gas flow of the oxygen, silane, and inert gas, of 625 sccm or less, or 500 sccm or less, using a high frequency bias signal power of 2000 watts or less, forming said first and second trenches with a width of 1800 Å to 3300 Å, and 6600 Å to 8800 Å, respectively, and forming the heights of said oxide-filled trenches being of 600 Å of reference top surfaces of the adjacent to silicon regions.

Liu et al discloses using oxygen, silane and inert gas to deposit a silicon oxide layer 52 over metal traces 48 by an HDP-CVD process (Column 4, lines 2-7), using a total gas mixture of oxygen, silane, and inert gas of 330 sccm (Column 4, lines 7-10), and using a high frequency bias signal power of 2000 watts (Column 4, lines 25-27). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chao et al and Liu et al, to enable the step of forming silicon dioxide layer 501 of Chao et al to be performed, and to provide an effective and very manufacturable method of depositing silicon dioxide between features in the manufacture of in integrated circuits (Liu et al, Column 2, lines 59-62).

It would have been a matter of routine optimization within the teachings of Chao et al to determine a suitable oxygen inflow rate to silane inflow rate ratio, a suitable high frequency bias signal power, suitable widths, and to determine a suitable height, to achieve the silicon oxide deposition step, the trenches formation step, and oxide-filled trenches formation step, of Chao et al to be performed.

In addition, the selection of a suitable oxygen inflow rate to silane inflow rate ratio, a suitable high frequency bias signal power, suitable widths, and suitable height, is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)(claimed ranges or a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In

re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill or art) and In re Aller, 105 USPQ 233 (CCPA 1995) (selection of optimum ranges within prior art general conditions is obvious).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruf*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Applicant argues that neither Chao et al nor Liu et al teach the use of an E/D ratio of about 0.07 or less during the filling of the trenches with different aspect ratios. However, as discussed above, Chao et al discloses controlling the sputter etch and deposition of the silicon

dioxide such that a nonzero etch to deposition ratio ranges from is 0.01 to 0.1 is established during the filling of said different trenches, wherein a 0.07, 0.025 or less etch to deposition ratio could be selected (Column 3, lines 40-43).

Claims 11, and 44-52, are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joannie García whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

JAG
November 8, 2004

GFourson
Primary Examiner